AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS

1. (cancelled)

2. (currently amended) ~~The differential amplifier according to claim 1~~ A differential amplifier comprising:

a differential amplifier circuit comprising first and second differential amplifier sections;

wherein said first differential amplifier section comprises:

a first differential pair of PMOS transistors which receives first and second input voltages, respectively;

wherein said second differential amplifier section comprises:

a second differential pair of NMOS transistors which receive said first and second input voltages, respectively;

a bias circuit which only activates only one of said first and second differential amplifier sections in response to a control signal; and

an output circuit which outputs an output signal from an output of said activated differential amplifier section,

wherein said first and second differential amplifier

sections comprise a first PMOS transistor and a first NMOS transistor function as constant current sources, respectively,

said bias circuit stops an operation of said first PMOS transistor when activating said second differential amplifier section, and stops an operation of said first NMOS transistor when activating said first differential amplifier section.

3. (original) The differential amplifier according to claim 2, wherein said bias circuit comprises:

a first switch arranged to connect a first bias voltage to a gate of said first PMOS transistor in response to said control signal; and

a second switch arranged to connect a second bias voltage to a gate of said first NMOS transistor in response to said control signal, and

when one of said first and second switches is turned on, the other is turned off.

4. (original) The differential amplifier according to claim 3, wherein said bias circuit comprises:

an inverter which inverts said control signal;

a third switch which is connected between said power supply line and the gate of said first PMOS transistor and switches in response to the inverted control signal; and

a fourth switch which is connected between said ground

line and the gate of said first NMOS transistor and switches in response to the inverted control signal,

when one of said third and fourth switches is turned on, the other is turned off.

4
~~5.~~ (original) The differential amplifier according to claim ~~1~~ 3, wherein when said first switch is turned on, said third switch is turned off, and when said second switch is turned on, said fourth switch is turned off.

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5
~~6.~~ (currently amended) ~~The differential amplifier according to claim 1~~ A differential amplifier comprising:

a differential amplifier circuit comprising first and second differential amplifier sections;

wherein said first differential amplifier section comprises:

a first differential pair of PMOS transistors which receives first and second input voltages, respectively;

wherein said second differential amplifier section comprises:

a second differential pair of NMOS transistors which receive said first and second input voltages, respectively;

a bias circuit which only activates only one of said first and second differential amplifier sections in response to a control signal; and

an output circuit which outputs an output signal from an output of said activated differential amplifier section,

wherein said first differential amplifier section comprises:

a first current mirror circuit whose input is connected with an output from one of said PMOS transistors of said first differential pair; and

a second current mirror circuit whose input is connected with an output from the other of said PMOS transistors of said first differential pair,

said second differential amplifier section comprises:

a third current mirror circuit, one of whose outputs is connected with one of said NMOS transistors of said second differential pair; and

a fourth current mirror circuit, one of whose outputs is connected with the other of said NMOS transistors of said second differential pair.

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6
~~7~~. (original) The differential amplifier according to claim 5~~6~~, wherein the other output of said third current mirror circuit is connected with the input of said second current mirror circuit, and

the other output of said fourth current mirror circuit is connected with the input of said first current mirror circuit.

7 ~~6~~. (original) The differential amplifier according to claim 6 ~~7~~, wherein said output circuit obtains the output of said activated differential amplifier section from said third and fourth current mirror circuits.

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8 ~~9~~. (currently amended) ~~The differential amplifier according to claim 1~~ A differential amplifier comprising:

a differential amplifier circuit comprising first and second differential amplifier sections;

wherein said first differential amplifier section comprises:

a first differential pair of PMOS transistors which receives first and second input voltages, respectively;

wherein said second differential amplifier section comprises:

a second differential pair of NMOS transistors which receive said first and second input voltages, respectively;

a bias circuit which only activates only one of said first and second differential amplifier sections in response to a control signal; and

an output circuit which outputs an output signal from an output of said activated differential amplifier section, and further comprising:

a control signal generating circuit which generates said control signal based on said first and second input

voltages.

9
10. (original) The differential amplifier according to PN
claim 8, wherein said control signal generating circuit comprises:

a first circuit which generates an average voltage of said first and second input voltages; and

a second circuit which generates said control signal from said average voltage.

10
11. (original) The differential amplifier according to claim 10, wherein said first circuit comprises:

a second constant current source connected with said ground line;

third NMOS transistors which are connected with said second constant current source and receives said first and second input voltages at gates of said third NMOS transistors;

fourth NMOS transistors which are connected with said second constant current source; and

a current mirror which is connected with said power supply line and supplies said fourth NMOS transistor with a current equal to a sum of currents flowing through said third NMOS transistors, and

said average voltage is outputted from a node between said current mirror and said fourth NMOS transistors.

11 ~~12~~. (original) The differential amplifier according to claim 10 ~~11~~, wherein said second circuit comprises:

a comparator which compares a predetermined reference voltage and said average voltage to output said control signal.

12 ~~13~~. (original) The differential amplifier according to claim 10 ~~11~~, wherein said control signal generating circuit further comprises:

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a filter circuit which is provided between said first and second circuits.

13 ~~14~~. (original) The differential amplifier according to claim 10 ~~11~~, wherein said first circuit further comprises:

a buffer which is connected between said node and said second circuit.

15. (cancelled)

14 ~~16~~. (currently amended) ~~The method according to claim 15~~ A method of outputting an output signal from first and second input voltages in an differential amplifier circuit comprising first and second differential amplifier sections, wherein said first differential amplifier section comprises a first differential pair of PMOS transistors which respectively receives first and second input voltages, and wherein said second

differential amplifier section comprises a second differential pair of NMOS transistors which respectively receives said first and second input voltages, said method comprising:

activating only one of said first and second differential amplifier sections in response to a control signal;

supplying first and second input voltages to said activated differential amplifier section; and

outputting an output signal from an output of said activated differential amplifier section,

wherein said activating comprises:

(a) controlling a first constant current source for said first differential amplifier section to be tuned on and a second constant current source for said second differential amplifier section to be turned off when said first differential amplifier section is activated in response to said control signal; and

(b) controlling said second constant current source to be turned on and said first constant current source to be turned off when said second differential amplifier section is activated in response to said control signal.

15 ~~17~~. (original) The method according to claim ~~16~~ 14, wherein said (a) controlling comprises:

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supplying a first bias voltage to a gate of a first PMOS transistor of said first constant current source; and

stopping the supply of said first bias voltage to the gate of said first PMOS transistor.

16 ~~18~~. (original) The method according to claim 14 ~~16~~, wherein said (b) controlling comprises:

supplying a second bias voltage to a gate of a first NMOS transistor of said second constant current source; and

stopping the supply of said second bias voltage to the gate of said first NMOS transistor.

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17 ~~19~~. (original) The method according to claim 14 ~~16~~, wherein said activating comprises:

inverting said control signal;

stopping an operation of said second constant current source in response to the inverted control signal, when said first differential amplifier section is activated in response to said control signal; and

stopping an operation of said first constant current source in response to the inverted control signal, when said second differential amplifier section is activated in response to said control signal.

18 ~~20~~. (currently amended) ~~The method according to claim 15, further comprising:~~ A method of outputting an output signal from first and second input voltages in an differential amplifier

circuit comprising first and second differential amplifier sections, wherein said first differential amplifier section comprises a first differential pair of PMOS transistors which respectively receives first and second input voltages, and wherein said second differential amplifier section comprises a second differential pair of NMOS transistors which respectively receives said first and second input voltages, said method comprising:

activating only one of said first and second differential amplifier sections in response to a control signal;

supplying first and second input voltages to said activated differential amplifier section;

outputting an output signal from an output of said activated differential amplifier section; and

generating said control signal based on said first and second input voltages.

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19

~~21~~. (currently amended) ~~The differential amplifier according to claim 1~~ A differential amplifier comprising:

a differential amplifier circuit comprising first and second differential amplifier sections;

wherein said first differential amplifier section comprises:

a first differential pair of PMOS transistors which receives first and second input voltages, respectively;

wherein said second differential amplifier section comprises:

a second differential pair of NMOS transistors which receive said first and second input voltages, respectively;

a bias circuit which only activates only one of said first and second differential amplifier sections in response to a control signal; and

an output circuit which outputs an output signal from an output of said activated differential amplifier section, and further comprising:

a first input voltage terminal; and

a second input voltage terminal, wherein,

said first differential pair of PMOS transistors have gates respectively connected to the first and second input voltage terminals, and

said second differential pair of NMOS transistors have gates respectively connected to the first and second input voltage terminals,

said first and second differential amplifier sections comprise a first PMOS transistor and a first NMOS transistor connected as constant current sources respectively to the first and second differential pair transistors, respectively, and

said bias circuit stops an operation of said first PMOS transistor when activating said second differential amplifier section, and stops an operation of said first NMOS transistor

when activating said first differential amplifier section.

20 ~~22~~. (currently amended) The differential amplifier according to claim [[1]] ~~2~~ 1, wherein only said first differential amplifier section is activated for a first predetermined time period and only said second differential amplifier section is activated for a second predetermined time period of time period different than the first predetermined time period.

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21 ~~23~~. (currently amended) ~~The differential amplifier according to claim 1~~ A differential amplifier comprising:

a differential amplifier circuit comprising first and second differential amplifier sections;

wherein said first differential amplifier section comprises:

a first differential pair of PMOS transistors which receives first and second input voltages, respectively;

wherein said second differential amplifier section comprises:

a second differential pair of NMOS transistors which receive said first and second input voltages, respectively;

a bias circuit which only activates only one of said first and second differential amplifier sections in response to a control signal; and

an output circuit which outputs an output signal from

an output of said activated differential amplifier section,

wherein only said first differential amplifier section is activated when a voltage level of a predetermined signal is closer to a higher power supply voltage and only said second differential amplifier section is activated when the voltage level of the predetermined signal is closer to a lower power supply voltage.

22 ~~24~~. (new) The differential amplifier according to claim 5 ~~8~~, wherein only said first differential amplifier section is activated for a first predetermined time period and only said second differential amplifier section is activated for a second predetermined time period of time period different than the first predetermined time period.

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23 ~~25~~. (new) The differential amplifier according to claim 8 ~~9~~, wherein only said first differential amplifier section is activated for a first predetermined time period and only said second differential amplifier section is activated for a second predetermined time period of time period different than the first predetermined time period.